MAMIDALA PALLAVI

	Name : M.Pallavi
	Designation : Assistant Professor
	Total Experience:4
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Specialization	Embedded systems & vlsi design
Academic Qualification	B.Tech / B.E. Details:ECE
	M.Tech / M.E. Details:Embedded systems & vlsi design
	PGDip:Physical desgining of ASIC
Total Teaching Experience	4.5
Publication Details	**International Journals:**
	A Low-Power Track and hold Amplifier with 55 GHz-Bandwidth" published in journal IJARTET volume 4,issue 3,march 2017
	"Optimized test compression for ultra-large-scale soc Architectures performing scan test bandwidth Management" published in journal IJMTER Volume 04, Issue 10, [October– 2017]
	Design of Low Power Adder in ALU Using Flexible Charge Recycling Dynamic Circuit" Published in journal IJR Volume 04 Issue 14 November 2017
	An Efficient Permanent Fault Detection Method in fifo buffers of NOC routers" published in journal IJETER volume5,issue11,Nov 2017.
	Design of FPGA logic architechtures using Hybrid/LUT Multiplexer" published in journal
	"Minimizing the Sub - Threshold Leakage for High Performance CMOS Circuits Using Stacked Sleep Technique published in international Journal of Electrical Engineering. ISSN 0974-2158 Volume 10, Number 3 (2017), pp. 323-335 © International Research Publication House
Awards & Honours	
	Toastmasters seminars in Hitam

MAMIDALA PALLAVI	
Workshops / Seminars / Conferences / Training Programs Attended	Seminar on professional awareness on vlsi jobs ieee cas /eds society in OU