DDTV Course outcomes

At the end of the course a student will be able to:

CO1: Define and describe digital design flows for system design recognizes the tradeoffs (Elective) involved in different approaches.

CO2: Describe, design, simulate and synthesize computer hardware using verilog HDL.

CO3: Know the fundamentals of verilog, with particular emphasis on synthesize constructs.

CO4: Develop digital systems in a hierarchical and module nature to aid testing, debugging and hardware reuse.

CO5: Design combinational, sequential logic and complex state machines (present in all practical computers).